Listing of Claims

1. (Currently Amended) A capacitor having a dielectric structure comprising:

a silicon carbide layer;

a first oxide layer having a first thickness directly on the silicon carbide layer;

a layer of dielectric material on the first oxide layer and having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

a second oxide layer on the layer of dielectric material opposite the first oxide layer and having a third thickness; and

wherein the first thickness is between about 0.5 and about 33 percent and the ~~second~~ third thickness is between about 0.5 and about 33 percent of the sum of the first, second and third thicknesses.

2. (Currently Amended) A capacitor having a dielectric structure comprising:

a silicon carbide layer;

a first oxide layer having a first thickness on the silicon carbide layer;

a layer of dielectric material on the first oxide layer and having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

a second oxide layer on the layer of dielectric material opposite the first oxide layer and having a third thickness;

wherein the first thickness ~~is between about 0.5 and about 33 percent~~ and the third ~~second~~ thickness ~~is between about 0.5 and about 33 percent of the sum of the first, second and~~ are an order of magnitude smaller than the second thickness ~~third thicknesses~~;

a first metal layer on the first oxide layer opposite the layer of dielectric material and disposed between the first oxide layer and the silicon carbide layer; and

a second metal layer on the second oxide layer opposite the high dielectric layer so as to provide a metal-insulator-metal (MIM) capacitor.

3. (Original) The capacitor of Claim 2, wherein the first oxide layer and the second oxide layer comprise silicon dioxide and wherein the layer of dielectric material comprises at least one of silicon nitride and silicon oxynitride.

4. Cancelled.

5. (Original) The capacitor of Claim 3, wherein the first thickness is from about 10 to about 30 nm, the second thickness is from about 200 to about 300 nm and the third thickness is from about 10 to about 30 nm.

6. (Original) The capacitor of Claim 3, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured so that the dielectric structure has a mean time to failure versus voltage characteristic which has a greater slope than a corresponding MIM capacitor with only a nitride dielectric.

7. (Original) The capacitor of Claim 3, wherein the silicon dioxide layers and the silicon nitride layer are deposited layers.

8. (Original) The capacitor of Claim 2, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

9. (Original) The capacitor of Claim 8, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of at least about 100 °C.

10. (Original) The capacitor of Claim 2, wherein the first and second metal layers comprise at least one of titanium, platinum, chromium and gold.

11. (Original) The capacitor of Claim 2, further comprising a silicon carbide substrate on which the capacitor is formed.

12. (Original) The capacitor of Claim 11, further comprising a plurality of semiconductor devices formed in the silicon carbide substrate.

13. (Currently Amended) A high mean time to failure interconnection structure for an integrated circuit, comprising:

a plurality of semiconductor devices in a substrate;

an insulating layer on the plurality of semiconductor devices;

a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;

a first layer of oxide on the first interconnect layer so as to cover at least a portion of the plurality of regions of interconnection metal;

a layer of dielectric material on the first layer of oxide opposite the first interconnect layer and having a dielectric constant higher than a dielectric constant of the first oxide layer;

a second layer of oxide on the layer of dielectric material opposite the first layer of oxide, wherein a thickness of the first layer of oxide and a thickness of the second layer of oxide are an order of magnitude smaller than a thickness of the layer of dielectric material; and

a second interconnect layer on the second layer of oxide opposite the layer of dielectric material and having a plurality of regions of interconnection metal.

14. (Original) The interconnection structure of Claim 13, wherein the first oxide layer and the second oxide layer comprise silicon dioxide layer and wherein the layer of dielectric material comprises silicon nitride.

15. (Original) The interconnection structure of Claim 14, wherein the first oxide layer has a thickness of from about 10 to about 30 nm, the layer of dielectric material has a thickness of from about 200 to about 300 nm and the second oxide layer has a thickness of from about 10 to about 30 nm.

16. Cancelled.

17. (Currently Amended) The interconnection structure of Claim ~~16~~13, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure versus voltage characteristic which has a greater slope than a corresponding nitride inter-metal dielectric.

18. (Original) The interconnection structure of Claim 14, wherein the silicon dioxide layers and the silicon nitride layer are deposited layers.

19. (Original) The interconnection structure of Claim 13, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

20. (Original) The interconnection structure of Claim 19, wherein at least one of the first oxide layer, the second oxide layer and the layer of dielectric material are configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of 150 °C.

21. (Original) The interconnection structure of Claim 13, wherein the interconnect metal of the first and second interconnect layers comprise at least one of titanium, platinum, chromium and gold.

22.-32. Cancelled.

33. (Previously Presented) A capacitor comprising:

a silicon carbide layer;

a layer of dielectric material on the silicon carbide layer, the layer of dielectric material comprising silicon oxynitride having a formula $Si_3N_{4-X}O_X$, where $0<X<1$;

a first metal layer on the layer of dielectric material opposite the silicon carbide layer; and

a second metal layer on the layer of dielectric material and disposed between the layer of dielectric material and the silicon carbide layer so as to provide a metal-insulator-metal (MIM) capacitor.

34. (Original) The capacitor of Claim 33, wherein the layer of dielectric material is configured so that the dielectric structure has a mean time to failure versus voltage characteristic which has a greater slope than a corresponding MIM capacitor with only a nitride dielectric.

35. (Original) The capacitor of Claim 33, wherein the silicon oxynitride of the layer of dielectric material is a deposited layer.

36. (Original) The capacitor of Claim 33, wherein the layer of dielectric material is configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

37. (Original) The capacitor of Claim 36, wherein the layer of dielectric material is configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of at least about 100 °C.

38. (Original) The capacitor of Claim 33, wherein the first and second metal layers comprise at least one of titanium, platinum, chromium and gold.

39. (Original) The capacitor of Claim 33, further comprising a plurality of semiconductor devices formed in the silicon carbide layer.

40. (Original) A high mean time to failure interconnection structure for an integrated circuit, comprising:

a plurality of semiconductor devices in a silicon carbide substrate;

an insulating layer on the plurality of semiconductor devices;

a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;

a layer of dielectric material on the first layer of oxide opposite the first interconnect layer, the layer of dielectric material comprising silicon oxynitride having a formula $Si_3N_{4-X}O_X$, where $0<X\leq 1$;

a second interconnect layer on the layer of dielectric material opposite the first interconnect layer and having a plurality of regions of interconnection metal.

41. (Original) The interconnection structure of Claim 40, wherein the layer of dielectric material has a thickness of from about 20 nm to about 400 nm.

42. (Original) The interconnection structure of Claim 40, wherein the layer of dielectric material is configured to provide a mean time to failure versus voltage characteristic which has a greater slope than a corresponding nitride inter-metal dielectric.

43. (Original) The interconnection structure of Claim 40, wherein the layer of dielectric material is a deposited layer of silicon oxynitride.

44. (Original) The interconnection structure of Claim 43, wherein the layer of dielectric material is configured to provide a mean time to failure of at least about 10^7 hours at a voltage of greater than about 50 volts and a temperature of at least about 100 °C.

45. (Original) The interconnection structure of Claim 44, wherein the layer of dielectric material is configured to provide a mean time failure of at least about 10^7 hours at a voltage of greater than about 100 volts and a temperature of 150 °C.

46. (Original) The interconnection structure of Claim 40, wherein the interconnect metal of the first and second interconnect layers comprise at least one of titanium, platinum, chromium and gold.

47.-56. Cancelled

57. (New) The capacitor of Claim 2, wherein the first thickness and the third thickness are at least six times smaller than the second thickness.

58. (New) The interconnection structure of Claim 13, wherein the thickness of the first layer of oxide and the thickness of the second layer of oxide are at least six times smaller than the thickness of the layer of dielectric.

59. (New) The capacitor of Claim 33, wherein the layer of dielectric material is configured to provide an operating voltage of at least 100V.

60. (New) The interconnection structure of Claim 40, wherein the plurality of semiconductor devices have an operating voltage of at least 100V and wherein the layer of dielectric material is configured to withstand the operating voltage of at least 100V.

61. (New) A high voltage capacitor having a dielectric structure comprising:

a silicon carbide layer;

a first oxide layer having a first thickness on the silicon carbide layer;

a layer of dielectric material on the first oxide layer and having a second thickness, the layer of dielectric material having a dielectric constant higher than the dielectric constant of the first oxide layer;

a second oxide layer on the layer of dielectric material opposite the first oxide layer and having a third thickness;

a first metal layer on the first oxide layer opposite the layer of dielectric material and disposed between the first oxide layer and the silicon carbide layer; and

a second metal layer on the second oxide layer opposite the high dielectric layer so as to provide a metal-insulator-metal (MIM) capacitor, the first thickness, the second thickness and the third thickness being configured to provide an operating voltage of at least 100V.

62. (New) A high mean time to failure interconnection structure for a high voltage integrated circuit, comprising:

a plurality of semiconductor devices in a substrate, the semiconductor devices having an operating voltage of at least 100V;

an insulating layer on the plurality of semiconductor devices;

a first interconnect layer having a plurality of regions of interconnection metal on the insulating layer opposite the plurality of semiconductor devices;

a first layer of oxide on the first interconnect layer so as to cover at least a portion of the plurality of regions of interconnection metal;

a layer of dielectric material on the first layer of oxide opposite the first interconnect layer and having a dielectric constant higher than a dielectric constant of the first oxide layer;

a second layer of oxide on the layer of dielectric material opposite the first layer of oxide; and

a second interconnect layer on the second layer of oxide opposite the layer of dielectric material and having a plurality of regions of interconnection metal

wherein the first layer of oxide, the second layer of oxide and the layer of dielectric material are configured to withstand the operating voltage of at least 100V.